IN THE CLAIMS

1 – 7. (canceled).

8. (original) An integrated circuit chip package comprising:

a metal substrate core;

the metal substrate core having at least two electrically isolated regions;

wherein at least one of the electrically isolated regions of the metal substrate core is coupled with a digital ground of an integrated circuit chip.

9. (original) The integrated circuit chip package of claim 8, further comprising:

input and output signals of the integrated circuit chip routed through the electrically isolated region of the metal substrate core that is coupled with the digital ground of the integrated circuit chip.

10. (original) The integrated circuit chip package of claim 9, wherein at least one other of the electrically isolated regions of the metal substrate core is coupled with an operating voltage rail of the integrated circuit chip.

11. (original) The integrated circuit chip package of claim 9, wherein at least one other of the electrically isolated regions of the metal substrate core is coupled with an analog ground of the integrated circuit chip.

12. (original) An integrated circuit chip package comprising:

a metal substrate core;

the metal substrate core having at least three electrically isolated regions;

wherein at least one of the electrically isolated regions of the metal substrate core is coupled with a digital ground of an integrated circuit chip and has input and output signals routed through it.

13. (original) The integrated circuit chip package of claim 12, wherein at least one other of the electrically isolated regions of the metal substrate core is coupled with an operating voltage rail of the integrated circuit chip.

14. (original) The integrated circuit chip package of claim 12, wherein at least one other of the electrically isolated regions of the metal substrate core is coupled with an analog ground of the integrated circuit chip.

15. (original) The integrated circuit chip package of claim 12, wherein at least one other of the electrically isolated regions of the metal substrate core is coupled with an operating voltage rail of the integrated circuit chip, and at least one other of the electrically isolated region of the metal substrate core is coupled with an analog ground of the integrated circuit chip.

16 – 20. (canceled).